In the Specification

Replace the paragraph beginning at page 1, line 4 with the following rewritten paragraph:

This is a continuation of application Serial Number 10/254,105 filed on September 24, 2002, which is a continuation of application Serial Number 09/896,687 filed on June 28, 2001, now U.S. Patent No. 6,457,073 which is a divisional of application Serial Number 09/471,217 filed on December 23, 1999, now U.S. Patent No. 6,260,082 which claims priority of provisional application Serial Number 60/113,555 filed on December 23, 1998, each of which is incorporated by reference herein in its entirety.

Replace the paragraph beginning at page 6, line 16 with the following re-written paragraphs.

Further details of a presently preferred ManArray core, architecture, and instructions for use in conjunction with the present invention are found in

U.S. Patent Application Serial No. 08/885,310 filed June 30, 1997, now U.S. Patent No. 6,023,753,

U.S. Patent Application Serial No. 08/949,122 filed October 10, 1997, now U.S. Patent No. 6,167,502,

U.S. Patent Application Serial No. 09/169,255 filed October 9, 1998, now U.S. Patent No. 6,343,356,

U.S. Patent Application Serial No. 09/169,256 filed October 9, 1998, now U. S. Patent No. 6,167,501,

U.S. Patent Application Serial No. 09/169,072, filed October 9, 1998, now U.S. Patent No. 6,219,776,

U.S. Patent Application Serial No. 09/187,539 filed November 6, 1998, now U.S. Patent No. 6,151,668,

U.S. Patent Application Serial No. 09/205,5588 filed December 4, 1998, now U.S. Patent No. 6,173,389,

U.S. Patent Application Serial No. 09/215,081 filed December 18, 1998, now U.S. Patent No. 6,101,592,

U.S. Patent Application Serial No. 09/228,374 filed January 12, 1999 now U.S. Patent No. 6,216,223, and entitled "Methods and Apparatus to Dynamically Reconfigure the Instruction Pipeline of an Indirect Very Long Instruction Word Scalable Processor",

U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, now U.S. Patent No. 6,366,999,

U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, now U.S. Patent No. 6,446,190,

U.S. Patent Application Serial No. 09/337,839 filed June 22, 1999,

U.S. Patent Application Serial No. 09/350,191 filed July 9, 1999, now U.S. Patent No. 6,356,994,

U.S. Patent Application Serial No. 09/422,015 filed October 21, 1999 entitled "Methods and Apparatus for Abbreviated Instruction and Configurable Processor Architecture", now U.S. Patent No. 6,408,382,

U.S. Patent Application Serial No. 09/432,705 filed November 2, 1999 entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding",

U.S. Patent Application Serial No. [[_____]] 09/472,372 filed December 23, 1999 entitled "Methods and Apparatus for Providing Direct Memory Access Control", now U.S. Patent No. 6,256,683, as well as,

Provisional Application Serial No. 60/113,637 entitled "Methods and Apparatus for Providing Direct Memory Access (DMA) Engine" filed December 23, 1998,

Provisional Application Serial No. 60/113,555 entitled "Methods and Apparatus Providing Transfer Control" filed December 23, 1998,

Provisional Application Serial No. 60/139,946 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 18, 1999,

Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999,

Provisional Application Serial No. 60/140,163 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 1999,

Provisional Application Serial No. 60/140,162 entitled "Methods and Apparatus for Initiating and Re-Synchronizing Multi-Cycle SIMD Instructions" filed June 21, 1999,

Provisional Application Serial No. 60/140,244 entitled "Methods and Apparatus for Providing One-By-One Manifold Array (1x1 ManArray) Program Context Control" filed June 21, 1999,

Provisional Application Serial No. 60/140,325 entitled "Methods and Apparatus for Establishing Port Priority Function in a VLIW Processor" filed June 21, 1999,

Provisional Application Serial No. 60/140,425 entitled "Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax" filed June 22, 1999,

Provisional Application Serial No. 60/165,337 entitled "Efficient Cosine Transform Implementations on the ManArray Architecture" filed November 12, 1999, and

Provisional Application Serial No. [[_____]] 60/171,911 entitled "Methods and Apparatus for DMA Loading of Very Long Instruction Word Memory" filed December 23, 1999, respectively, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.